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PATENT
Docket No. Intel/17880

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Patel et al.

Serial No.: 10/747,764

Filed: December 29, 2003

For: Methods and Apparatus for Address Generation in Processors

Group Art Unit: 2183

Examiner: Not yet assigned

I hereby certify that this paper is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this date:

June 22, 2004

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INFORMATION DISCLOSURE STATEMENT

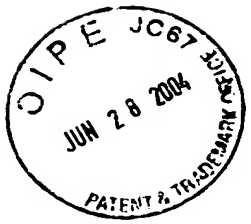
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The publications listed on the enclosed PTO Form-1449 are submitted pursuant to 37 CFR §§ 1.56, 1.97, and 1.98. Copies of the publications are enclosed.

TIME OF FILING

This information disclosure statement is being filed, to the best of the undersigned's knowledge, before the mailing date of a first Office action on the merits. In accordance with 37 CFR §1.97(b), no certification or fee is required.



METHOD OF PAYMENT

No fee is required.

The Commissioner is authorized to charge any fee deficiency required by this paper, or credit any overpayment, to Deposit Account No. 50-2455. A copy of this paper is enclosed.

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Respectfully submitted,

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June 22, 2004

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Form PTO-1449 (Modified)	U.S. Department of Commerce Patent and Trademark Office	Atty. Docket No. Intel/17880	Serial No. 10/747,764
INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)		Applicants Patel et al.	
		Filing Date **December 29, 2003**	Group Art Unit 2183

		OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)
	C01	*P6 Family of Processors: Hardware Developer's Manual,* Intel Corporation, September 1998, 16 pages
	C02	*IS 32 Intel Architecture Software Developer's Manual*, Volume 3: System Programing Guide, Intel Corporation, 2003, Chapter 2: Sytem Architecture Overview, pp. 2.1-2.7
	C03	*IS 32 Intel Architecture Software Developer's Manual,* Volume 3: System Programing Guide, Intel Corporation, 2003, Chapter 3: Protected-Mode Memory Management, pp. 3.1-3.38
	C04	*IA-32 Intel® Architecture Optimization:* Reference Manual, Intel Corporation, 2003, Chapter 1: IA-32 Intel® Architecture Processor Family Overview, pp. 1.1- 1-34
	C05	*IA-32 Intel® Architecture Software Developer's Manual,* Volume 1: Basic Architecture, Intel Corporation, 2003, Chapter 3: Basic Execution Environment, pp. 3.1-3.17

EXAMINER	DATE CONSIDERED
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	